Course Outline:

This is a half day workshop that provides system architects, DSP designers, and FPGA designers a hands-on course covering how to develop Xilinx design flow for implementing DSP functions using System Generator. The course will be organized on:

Date: 26-Mar 2010
Time: 2-5pm.
Venue: UTAR Setapak.

Actual room will be informed prior to the seminar.

You will learn how to:

1) Use Simulink to perform system-level DSP design

2) Approach the complexities of high-performance DSP design

3) Implement a design from algorithm concept to hardware verification using Xilinx automatic translation (System Generator)

This course allows you to explore the System Generator tool and to gain the expertise you need to develop advanced, low-cost DSP designs. This intermediate course in implementing DSP functions focuses on learning how to use System Generator for DSP, design implementation tools, and hardware-in-the-loop verification. Through hands-on exercises, you will implement a design from algorithm concept to hardware verification by using Xilinx FPGA capabilities.

* Introduction to System Generator

* Simulink Basics

* Using Simulink - Basic Xilinx Design Capture

* Getting Started with Xilinx System Generator - Signal Routing

* Signal Routing - Implementing System Control

* Implementing System Control - Multi-Rate Systems

* Filter Design
For those who are interested, please contact for the registration: Mr. Chan Kim Chon (chankc@utar.edu.my).